METHOD AND SYSTEM FOR CONTROLLING THE DUTY CYCLE OF A CLOCK SIGNAL

Abstract Of The Disclosure

A system for controlling the duty cycle of a clock signal. The system includes a duty cycle adjustment circuit that receives an input clock signal and generates an output clock signal. The duty cycle adjustment circuit charges a capacitor when the input clock signal has a first logic level and discharges the capacitor with the input clock signal has a second logic level. The rates of charge and discharge are controlled by first and second control signals. When the capacitor has been charged to a first transition level, the output clock signal transitions to a first logic level, and when the capacitor has been discharged to a second transition level, the output clock signal transitions to a second logic level. The first and second control signals are supplied by a feedback circuit, which is implemented using an integrator circuit that receives the output clock signal and generates a feedback signal indicative of the duty cycle of the output clock signal. A transconductance amplifier compares the feedback signal to a reference voltage, and generates first and second currents corresponding thereto. These currents are converted to the first and second control signals by a control circuit, which includes a current mirror. The control circuit provides good immunity from power supply fluctuations.